REMARKS

This amendment responds to the office action mailed on May 10, 2002. In the office action the Examiner:

* rejected claims 32, 38, 44, 47, and 51-65 under 35 U.S.C. 112, second paragraph, as indefinite;

* rejected claims 1, 3-5, 28, 29, 33, 34, 54, 56, 58, and 60-65 under 35 U.S.C. 103(a) as being unpatentable over Char et al. (5,157,466) in view of Ishimaru et al. (5,883,051);

* rejected claims 2, 30, 31, and 52 under 35 U.S.C. 103(a) as being unpatentable over Char et al. (5,157,466) in view of Ishimaru et al. (5,883,051) and further in view of Shnirman et al. (Physical Review B 57, p. 15400, 1998);

* rejected claims 6, 8-10, 35, 39, 40, 41, 53, 55, 57, and 59 under 35 U.S.C. 103(a) as being unpatentable over Char et al. in view of Ishimaru et al. (5,883,051) and further in view of Baechtold et al. (3,953,749); and

* rejected claims 7, 11, 12-18, 36, 37, 42, 43, 45, 46, and 48-50 under 35 U.S.C. 103(a) as being unpatentable over Char et al. in view of Ishimaru et al. (5,883,051), Baechtold et al. (3,953,749), and further in view of Shnirman et al. (Physical Review B 57, p. 15400, 1998);

After entry of this amendment, the pending claims are claims 1-18 and 28-65.

Rejection of Claims Under 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 32, 38, 44, 47, and 51-65 under 35 U.S.C. 112, second paragraph, for four reasons. First, the Examiner contends that the meaning of the parity key, as recited in claims 32, 38, 44, 47, 51, and 61, is not clear. Second, the Examiner contends that is not clear where the clockwise and counterclockwise supercurrents recited in claims 52-55 are circulating. Third, the Examiner contends that the meaning of the term "twice degenerate states", as recited in claims 56-59, is not clear. Fourth, the Examiner contends that the tunneling between degenerate states recited in claims 60 and 64 is not clear. Applicant addresses each rejection in turn.

PARITY KEYS

Claims 32, 38, 44, 47, and 51-65 have been rejected under 35 U.S.C. 112, second paragraph for reciting the term "parity key." Applicant respectfully traverses

11090-003-999
Page 3
Amendment   CA1:311118.1

the rejection. To answer the question posed by the Examiner in the May 10, 2002 office action, the term "parity key" does not mean the "parity check" that is commonly found in computer science arts. On page 13 of Applicant's March 1, 2002 response to the October 1, 2001 office action, Applicant indicated that a parity key is a special form of a single-electron transistor (SET). In the October 1, 2001 office action, the Examiner rejected claim 15 under 35 U.S.C. 112, first paragraph, on the contention that the structure of a SET is not known. To respond to this rejection, Applicant discussed the fabrication, design, and function of SETs on pages 11 and 12 of the March 1, 2002 response. In the May 10, 2002 office action, the term SET was no longer rejected under 35 U.S.C. 112, first paragraph.

As is well known in the art, a parity key is a superconducting SET. The parity key only passes Cooper pairs (pairs of electrons), and only at certain gate voltages. The reference GL, which was submitted in the March 21, 2002 information disclosure statement, describes the physical properties of parity keys. (P. Joyez et al., "Observation of Parity-Induced Suppression of Josephson Tunneling in the Superconducting Single Electron Transistor", Physical Review Letters, Vol. 72:15, 2458-2461, April 11, 1994). Reference GL was incorporated by reference on page 15, line 17, of the specification.

The specification clearly illustrates the structure, function and use of parity keys. For example, page 14, lines 23-24, of the specification states that element 640 of Fig. 6 is a parity key or a SET. Inspection of Figure 6 shows that the structure of a parity key is clearly illustrated. Furthermore, to show that the term "parity key" is well known in the art, Applicant provides the reference Blais and Zagoskin, arXiv:quant-ph/9905043 v.2 (April 7, 2000) as Appendix C. In the last paragraph of column 1, the reference defines a parity key as a superconducting SET. Furthermore, Fig. 1a of the reference shows five parity keys, each designated "PK". The reference further refers to two other references for additional disclosure on the physical properties of SETs. One of the two references cited is reference GL submitted in the March 21, 2002 information disclosure statement. The other reference cited is Matveev et al., "Parity-induced suppression of the Coulomb blockade of Josephson tunneling," Phys. Rev. Lett. 70, 2940 (1993). If desired, the Applicant can provide additional references to refer to "parity keys" in order to establish that the term "parity key" as recited in claims 32, 38, 44, 47, and 51-65 particularly point out and distinctly claim Applicant's invention.

11090-003-999
Page 4
Amendment   CAI:311118.1

CLOCKWISE AND COUNTERCLOCKWISE SUPERCURRENTS

The Examiner has rejected claims 52-55 on the contention that these claims recite a clockwise or counterclockwise circulating supercurrent without specifying where these supercurrents are circulating. Applicant has amended claims 52-55 to recite that supercurrents are circulating in a plane in the vicinity of the clean Josephson junction. Support for this amendment is found on page 6, lines 25-29, and page 9, lines 8-12, of the specification as well as Figure 1A. In particular Fig. 1A shows a circle with arrows to indicate the path of one such supercurrent. In some embodiments of the invention that are encompassed by claims 52-55, the island or the bank is made of a d-wave superconductor and the clockwise and/or counter clockwise supercurrent flows in the ab-plane of the d-wave material. See specification, page 6, lines 21-28. The orientation of the ab plane, in accordance with some embodiments of the invention, is shown in Figures 1B and 1C.

TWICE DEGENERATE STATES

The Examiner contends that the meaning of the term "twice degenerate states," as recited in claims 56-59, is not clear. Applicant traverses the rejection. Claims 56-59 recite a quantum state of a qubit. These claims further recite that this quantum state is twice degenerate. The twice degenerate state recited in claims 56-59 refers to a qubit having two stable energy states each having the same energy. With reference to Fig 1A, page 9, lines 8-12 states:

> Two degenerate states having the ground state energy and
> definite magnetic moment correspond to minimal supercurrents
> circulating through Josephson junction 130 in clockwise and
> counterclockwise senses, in a preferred plane of the crystal structures
> of bank 110 and/or island 120.

Thus, in the embodiment illustrated in Fig. 1A, one of the degenerate states refers to the supercurrent flowing in the clockwise direction and the other degenerate state refers to the supercurrent flowing in the counterclockwise direction in a preferred plane of the island or the bank.

Further clarity on the recitation of the term "doubly degenerate is found on page 6, lines 21-28, of the specification:

> With a d-wave superconductor on at least one side of the Josephson junction, the Josephson junction has non-zero ground state supercurrent in the vicinity of the junction. This ground state supercurrent is either clockwise or counterclockwise in the preferred (so called ab-) plane of the d-wave superconductor. The ground state supercurrent in the vicinity of each Josephson junction is thus doubly degenerate and provides the basis for a quantum coherer or a qubit for quantum computing in accordance with an embodiment of the invention.

This passage clearly shows that claims 56-59 are particularly pointing out and distinctly claiming the subject matter that Applicant regards as his invention.

The concept of degenerate energy states is well known in the field of quantum mechanics. Degenerate level is defined in *Dictionary of Physics*, Longman, Singapore, 1958 as "An energy level of a quantum mechanical system that corresponds to more than one quantum state." Applicant provides the reference as Appendix D. A twice-degenerate state illustrated as a potential energy diagram is provided in Figure 1.
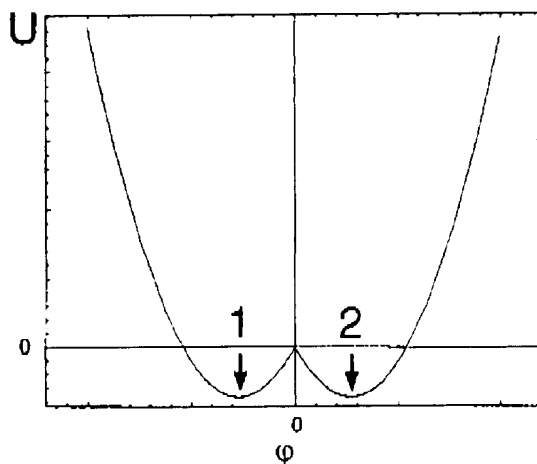

FIGURE 1

In Figure 1, "1" and "2" describe two potential energy wells in a potential energy diagram for the qubit recited in claims 56-59. As illustrated, states "1" and "2" are degenerate because the energies of the two states are the same. State "1" may represent the clockwise supercurrent and state "2" may represent the counterclockwise supercurrent that circulates across the Josephson junction as illustrated in Fig. 1A.

TUNNELING BETWEEN DEGENERATE STATES

The Examiner has rejected claims 60 and 64 because they recite the phrase "tunneling" within the limitation "quantum tunneling between the first ground state and the second ground state of the supercurrent associated with each Josephson junction." The first ground state and the second ground state of the system recited in claims 60 and 64 correlate with circulation directions of the supercurrent. For example, using Figure 1 above as a reference, the energy states "1" and "2" could represent the first ground state and the second ground state of the system. The term "quantum tunneling" refers to the phenomena in which the system shifts from state "1" to state "2" or vice versa.

To establish that the term "quantum tunneling" is an art recognized expression, Applicant provides the reference Mooij *et al.*, 1999, "Josephson Persistent Current Qubit," Science 285, pp. 1036-1039 as Appendix E. Mooij *et al.* is reference IK submitted in the March 21, 2002 information disclosure statement. On page 1037, column 2, of the reference, it is states that "The barrier of quantum tunneling between the states depends strongly on the value of α." Without elaborating on the meaning of α within the context of the Mooij *et al.* reference, the reference establishes that the phrase "quantum tunneling" is a well-defined art accepted term. Accordingly, the Examiner's rejection of the term "tunneling" as recited in claims 60 and 64 is improper and the Applicant respectfully requests that the rejection be withdrawn.

DOUBLE PATENTING REJECTION

The Examiner provisionally rejected claims 1-18 and claims 28-65 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of copending application 09/855,817. Applicant traverses the rejection. The rejection is improper as a matter of law. The third sentence of 35 U.S.C. 121 states:

> A patent issuing on an application with respect to which a requirement for restriction under this section has been made, or on an application filed as a result of such a requirement, shall not be used as a reference either in the Patent and Trademark Office or in the courts against a divisional application or against the original application or any patent issued on either of them, if the application is filed before the issuance of the patent on the other application.

Copending application 09/855,817 is a divisional application of the present application. On February 23, 2001, the Examiner imposed a restriction requirement between Group I (claims 1-18 drawn to a quantum computing structure) and Group II (claims 19-27 drawn to a process). On March 16, 2001, Applicant elected without traverse to have the invention of Group I (claims 1-18) examined. All presently pending claims are drawn to a quantum computing structure and are thus properly classified as Group I claims in accordance with the February 23, 2001 restriction requirement.

On May 14, 2001, divisional application 09/855,817 was filed. The preliminary amendment, filed with application 09/855,817, cancelled claims 1-18. Thus, all that was pending in the divisional application was the claims of Group II as defined in the February 23, 2001 restriction requirement (claims 19-27). Although subsequent prosecution in the 09/855,817 application has resulted in additional pending claims in that application, each of the new pending claims is properly classified as a Group II claim in accordance with the February 23, 2001 restriction requirement. Therefore, 35 U.S.C 121, third sentence prohibits the Examiner from using application 09/855,817 as a reference for a double patenting rejection.

The 35 U.S.C. 121, third sentence, bar to double patenting rejections is also found in Section 804.01 of the M.P.E.P. (Original Eight Edition, August, 2001) which states in relevant part:

> The third sentence of 35 U.S.C. 121 prohibits the use of a patent issuing on an application with respect to which a requirement for restriction has been made, or on an application filed as a result of such a requirement, as a reference against any divisional application, if the divisional application is filed before the issuance of the patent.

Because the Examiner's double patenting rejection is erroneous both as a matter of a law and as a matter of patent examining procedure, Applicant respectfully requests that the rejection be withdrawn.

Rejection of Claims Under 35 U.S.C. 103(a)

The Examiner has rejected claims 1, 3-5, 28, 29, 33, 34, 54, 56, 68 and 60-65 under 35 U.S.C. 103(a) as being unpatentable over Char et al. (USP 5,157,466) in view of Ishimaru et al. (USP 5,883,051).

The Examiner bases the rejection on the contention that it would have been obvious to make part of the structure taught by Char *et al.* mesoscopic (*e.g.*, 310 of Char *et al.* Fig. 14) as a design alternative in view of the five micron neck disclosed in Ishimaru *et al.* The rejection is respectfully traversed. First, Char *et al.* does not teach or suggest an island. Second, there is no suggestion or motivation to modify or combine the teachings of Char *et al.* and Ishimaru *et al.* in order to achieve the claimed invention. Third, even if the failure to identify a suggestion or motivation to combine such references were overlooked, the combined structure would still not have a mesoscopic island as recited in independent claims 1, 28, 60 and 64. It is simply not possible for a five-micron wide bank to support discrete quantum states (*i.e.*, to be mesoscopic). Thus, contrary to the Examiner's contention, the devices in Char *et al.* cannot be made mesoscopic as a design alternative. These grounds for traversal will now be addressed in turn.

With respect to the first ground for traversal, the Examiner contends that Char *et al.* teaches the formation of a grain boundary JJ of high temperature superconductor material where a region 310 is connected to a body 312. Applicant respectfully submits that region 310 is not an island, much less a mesoscopic island. Rather, region 310 is a lead of a dc Superconducting Quantum Interference Device (SQUID). A dc SQUID can be made by patterning a superconducting thin film using photolithography to create parallel Josephson junctions as shown in Figure 2 below. In Char, current flows in one end of the dc SQUID and out the other end of region 310.
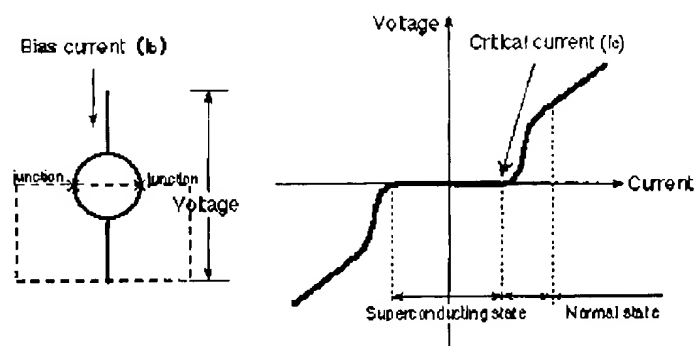
FIGURE 2

When bias current (Ib) is applied to the SQUID, voltage through the SQUID is zero when the current is less than the critical current of the Josephson junctions. When bias current exceeds critical current (Ic), the SQUID turns to the normal state and voltage is produced. Element 310 (Fig. 14 of Char *et al.*) refers to the entire portion of the circuit enclosed in the dashed box in Figure 2 above. This can be seen by inspection of Figure 14. In Figure 14, line 314 defines the grain boundary between regions 310 and 312. The two Josephson junctions found in a dc SQUID form an interface 314 between sections 312 and 310 at points 1000-1 and 1000-2 in the reproduction of Char *et al.*, Figure 14 below:
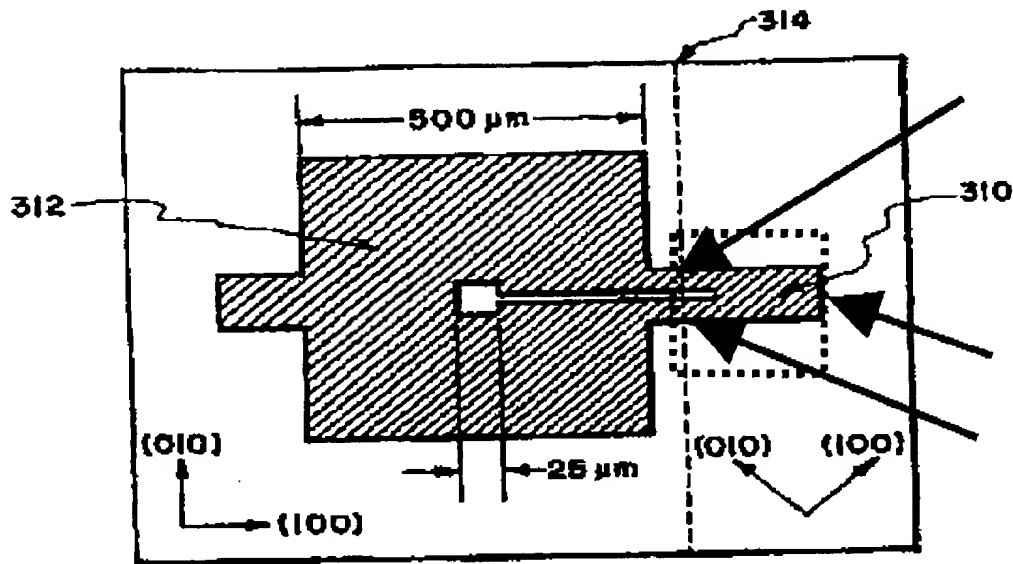
FIG. 14

Thus, the boxed region 1002 in the reproduction of Char *et al.* Fig. 14 is the same as the boxed region in Figure 2 above. As such, region 310 is not an island, but rather an electronic lead as well as an interface with two Josephson junctions (1000-1 and 1000-2).

With respect to the second ground for traversal, no motivation to combine references, the Examiner admits that Char *et al.* does not teach or suggest making part of the devices disclosed in Char *et al.* mesoscopic. To remedy this deficiency in Char *et al.*, the Examiner identifies a neck in Ishimaru *et al.* that is five microns wide. The Examiner states that, in view of the five-micron neck in Ishimaru *et al.*, it would have been obvious to make part of the Char *et al.* structure mesoscopic as a design alternative. However, there is absolutely no motivation to incorporate the five-micron dimension into the Char *et al.* device. If region 310 of the dc SQUID illustrated in Figure 14 of Char *et al.* were made mesoscopic, it would not improve the function of the dc SQUID. The mere fact that references can be modified or combined does not render the resultant modification or combination obvious unless the prior art also suggests the desirability of the modification or combination. MPEP § 2143.01. Here, there is no suggestion in Ishimaru *et al.* or Char *et al.* that such a modification would be desirable. In fact, if Char *et al.* and Ishamaru *et al.* were combined, the resultant combination would be inoperable/impractical. That is, the teachings of Ishimaru *et al.* result in current densities at least one order of magnitude smaller than those desired

by Char et al. (Char et al., column 3, lines 12-19, discussing 1×10^6 amperes/cm^2). Therefore, there is clearly no motivation, even as a design alternative, to combine Char et al. and Ishimaru et al.

Thirdly, even if lack of a suggestion or motivation to combine Char et al. and Ishimaru et al. and the failure of Char et al. to teach an island were overlooked, the combination of Char et al. and Ishimaru et al. would still not include a mesoscopic island. Yet, a mesoscopic island is recited in claims 1, 28, 60 and 64. Ishimaru et al. merely teaches patterning at the five-micron level. But it is simply not possible for a five-micron wide bank to support discrete quantum states (i.e., to be mesoscopic). In describing an exemplary embodiment, page 7, line 29, through page 8, line 2, of the specification details a mesoscopic island (Fig. 1A, element 120) having a width W (specification, Fig. 1A) of about 0.2 microns or less, a length L (specification, Fig. 1A) of about 0.5 microns or less, and a thickness of about 0.2 microns or less. The amount of capacitance stored by an island is a function of the width W (as shown in Fig. 1A of the instant application) of the island. A material having a width W on the order of five microns would have too much capacitance to be mesoscopic. No materials have been discovered to date that can support a mesoscopic system having a width W of five microns. Therefore, the combination of Char et al. and Ishimaru et al. does not teach or suggest a mesoscopic island as recited in claims 1, 28, 60 and 64.

For the three reasons identified above, Char et al., either alone or in combination with Ishimaru et al., does not anticipate claims 1, 28, 60 or 64. Because claims 3-5, 29, 33, 34, 54, 56, 58, 61-63, and 65 ultimately depend from claims 1, 28, 60 and 64, Char et al. in view of Ishimaru et al. does not anticipate these claims either.

Rejection of Claims Under 35 U.S.C. 103(a) Over Char et al. in View of Ishimaru et al. and further in view of Shnirman et al.

The Examiner has rejected claims 2, 30, 31, and 52 under 35 U.S.C. 103(a) as being unpatentable over Char et al. (USP 5,157,466) in view of Ishimaru et al. (USP 5,883,051) and further in view of Shnirman et al. (Physical Review B 57, 15400, 1998). Char et al., either alone or in combination with Ishimaru et al., does not anticipate claims 1, 28, 60 or 64 for the reasons discussed above. Shnirman merely teaches a SET coupled capacitively to a Josephson junction q-bit. As such, Shnirman et al. does not remedy the deficiencies identified in the combination of Char et al. and

11090-003-999
Page 12
Amendment

Ishimaru *et al.* For this reason, the combination of Char *et al.*, Ishimaru *et al.*, and Shnirman *et al.* does not render claims 1, 28, 60 or 64 obvious. Since claims 2, 30, 31, and 52 ultimately depend from 1, 28, 60 or 64, Char *et al.* in view of Ishimaru *et al.* and further in view of Shnirman *et al.* does not anticipate these claims either.

Rejection of Claims Under 35 U.S.C. 103(a) Over Char et al. in View of Ishimaru et al. and further in view of Baechtold et al.

The Examiner has rejected claims 6, 8-10, 35, 39, 40, 41, 53, 55, 57, and 59 under 35 U.S.C. 103(a) as being unpatentable over Char *et al.* (USP 5,157,466) in view of Ishimaru *et al.* (USP 5,883,051) and further in view of Baechtold *et al.* (USP 3,953,749). Char *et al.*, either alone or in combination with Ishimaru *et al.*, does not anticipate claims 1, 28, 60 or 64 for the reasons discussed above. Baechtold *et al.* merely teaches a binary circuit consisting of a series/parallel arrangement of Josephson junctions. As such, Baechtold *et al.* does not remedy the deficiencies identified in the combination of Char *et al.* and Ishimaru *et al.* For this reason, the combination of Char *et al.*, Ishimaru *et al.*, and Baechtold *et al.* does not render claims 1, 28, 60 or 64 obvious. Since claims 6, 8-10, 35, 39, 40, 41, 53, 55, 57, and 59 ultimately depend from 1, 28, 60 or 64, Char *et al.* in view of Ishimaru *et al.* and further in view of Baechtold *et al.* does not anticipate these claims either.

Rejection of Claims Under 35 U.S.C. 103(a) Over Char et al. in View of Ishimaru et al. and further in view of Baechtold et al. as well as Shnirman et al.

The Examiner has rejected claims 7, 11, 12-18, 36, 37, 42, 43, 45, 46, and 48-50 under 35 U.S.C. 103(a) as being unpatentable over Char *et al.* in view of Ishimaru *et al.* and further in view of Baechtold *et al.* as well as Shnirman *et al.* As previously discussed Char *et al.*, either alone or in combination with Ishimaru *et al.*, does not anticipate claims 1, 28, 60 or 64. Baechtold *et al.* and Shnirman *et al.* do not remedy the deficiencies identified in the combination of Char *et al.* and Ishimaru *et al.* For this reason, the combination of Char *et al.*, Ishimaru *et al.*, Baechtold *et al.*, and Ishimaru *et al.* does not render claims 1, 28, 60 or 64 obvious. Since claims 7, 11, 12-18, 36, 37, 42, 43, 45, 46, and 48-50 ultimately depend from claims 1, 28, 60 or 64, the combination of all four references does not anticipate these claims either.

In light of the above remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

PENNIE & EDMONDS LLP

By:_____
Gary S. Williams
Reg. No. 31,066

3300 Hillview Avenue
Palo Alto, CA 94304
Telephone: (650) 493-4935

11090-003-999
Page 14
Amendment

CA1 311118 1

APPENDIX A
CHANGES TO THE CLAIMS

The rewritten claims were revised as follows:

52. (Amended) The structure of claim 1, wherein a qubit is formed by the first bank, the mesoscopic island and the clean Josephson junction, and wherein each quantum state on the qubit is characterized by a clockwise or a counterclockwise [circulating] supercurrent that circulates in a plane in the vicinity of the clean Josephson junction.

53. (Amended) The quantum register of claim 8, wherein a plurality of qubits is formed by the plurality of mesoscopic islands, the bank, and the plurality of clean Josephson junctions, and wherein each quantum state on each respective qubit in said plurality of qubits is characterized by a clockwise or a counterclockwise [circulating] supercurrent that circulates in a plane in the vicinity of the Josephson junction in said respective qubit.

54. (Amended) The qubit of claim 28, wherein each quantum state on the qubit is characterized by a clockwise or a counterclockwise [circulating] supercurrent that circulates in a plane in the vicinity of the clean Josephson junction.

55. (Amended) The quantum register of claim 39, wherein a qubit is formed by each mesoscopic island in the at least one mesoscopic island together with the first bank and a Josephson junction in the at least one Josephson junction, and wherein each quantum state of each said qubit is characterized by a clockwise or a counterclockwise [circulating] supercurrent that circulates in a plane in the vicinity of the Josephson junction in said qubit.

11090-003-999
Page 15
Amendment

CA1:311118.1